



PTO/SB/08B (08-03)  
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| <b>Substitute for form 1449/PTO</b><br><br><b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br><br>(Use as many sheets as necessary) |      | <b>Complete if Known</b> |                      |
|  |      | Application Number       | 10/708,268           |
|  |      | Filing Date              | 02/20/2004           |
|  |      | First Named Inventor     | Praveen K. Samudrala |
|  |      | Art Unit                 | 2816 2814            |
|  |      | Examiner Name            | Unassigned           |
| Sheet 1  | of 1 | Attorney Docket Number   | 1372.136.PRC         |

| NON PATENT LITERATURE DOCUMENTS |                       |   |                |
|---------------------------------|-----------------------|---|----------------|
| Examiner Initials*              | Cite No. <sup>1</sup> | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T <sup>2</sup> |
| DC                              | 1                     | SAMUDRALA, PRAVEEN KUMER ET AL., Selective Triple modular Redundancy for SEU Mitigation in FPGAs, pgs 1-3, <i>no date</i>   |                |
| DC                              | 2                     | SAMUDRALA, PRAVEEN K. ET AL., Selective Triple Modular Redundancy (STMR) Based Single Event Upset (SEU) Tolerant Synthesis for FPGAs, pgs 1-26, <i>10/2004</i>  |                |
| DC                              | 3                     | SAMUDRALA, PRAVEEN K. ET AL., A Novel Technique for SEU Mitigation in Combinational Circuits Mapped to FPGA's, pgs 1-31.  |                |
| DC                              | 4                     | CARMICHAEL, CARL, Triple Module Redundancy Design Techniques for Virtex FPGAs, XILINX, Nov. 1, 2001, pgs 1-37, XAPP197 (v1.0).  |                |
| DC                              | 5                     | LABEL, KENNETH A. ET AL., Single-Event-Effect Mitigation from a System Perspective, IEEE Transactions on Nuclear Science, April 1996, 46-2, pp. 658-660   |                |
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|                    |                     |                 |                 |
|--------------------|---------------------|-----------------|-----------------|
| Examiner Signature | <i>David D. Chy</i> | Date Considered | <i>12/29/0x</i> |
|--------------------|---------------------|-----------------|-----------------|

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<sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> Applicant is to place a check mark here if English language Translation is attached.

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STATEMENT BY APPLICANT**

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Sheet 1 of 2

# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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|-------|---|----|---|
| Sheet | 1 | of | 2 |
|-------|---|----|---|

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| First Named Inventor   | Praveen K. Samudrala   |
| Art Unit               | <del>2848</del> - 2819 |
| Examiner Name          | Unassigned             |
| Attorney Docket Number | 1372.136.PRC           |

## U. S. PATENT DOCUMENTS

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| FOREIGN PATENT DOCUMENTS       |     |
|--------------------------------|-----|
| Publication                    | No. |
| 1. <i>U.S. Pat. 2,800,000</i>  | 1   |
| 2. <i>U.S. Pat. 2,800,001</i>  | 2   |
| 3. <i>U.S. Pat. 2,800,002</i>  | 3   |
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| 91. <i>U.S. Pat. 2,800,090</i> | 91  |
| 92. <i>U.S. Pat. 2,800,091</i> | 92  |
| 93.                            |     |

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| Examiner<br>Signature | <i>[Signature]</i> | Date<br>Considered | 12/28/0x |
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| First Named Inventor   | Praveen K. Samudrala |
| Art Unit               | 2816 - 2819          |
| Examiner Name          | Unassigned           |
| Attorney Docket Number | 1372.136.PRC         |

Sheet 2 of 2

**NON PATENT LITERATURE DOCUMENTS**

| Examiner Initials* | Cite No. <sup>1</sup> | Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published. | T <sup>2</sup> |
|--------------------|-----------------------|---|----------------|
| DC                 | 1                     | EDUARDO AUGUSTO BEZERRA ET AL., Improving Reconfigurable Systems Reliability by Combining Periodical Test and Redundancy Techniques: A Case Study, <i>pp. 1-10, no date</i>   |                |
| DC                 | 2                     | ZOLTAN MEGGYESI ET AL., FPGA Design in the Presence of Single Event Upsets, CERN, Geneva, Switzerland. <i>pp. 1-4, no date</i>  |                |
| DC                 | 3                     | Single Event Upset (SEU) Mitigation by Virtual Triple Modular Redundancy (TMR) in Design Reduces Manufacturing Cost and Lowers Power, Alternative System Concepts, Inc., pg. 1-7, <i>no date</i>  |                |
| DC                 | 4                     | EARL FULLER ET AL., Radiation Testing Update, SEU Mitigation, and Availability Analysis of the Virtex FPGA for Space Reconfigurable Computing, pg. 1-11, <i>9/2000</i>  |                |
| DC                 | 5                     | K. NIKOLIC ET AL., Fault-Tolerant Techniques for Nanocomputers, TNT2001, Sept. 3-7, 2001, Segovia, Spain, <i>pp. 1-3</i>  |                |
| DC                 | 6                     | CARL CARMICHEAL ET AL., SEU Mitigation Techniques for Virtex FPGAs in Space Application, <i>pp. 1-11, no date 1999</i>  |                |
| DC                 | 7                     | PRAVEEN SAMUDRALA ET AL., Single Event Upsets and Mitigation Techniques: A Survey, pages 1-15, <i>no date</i>   |                |
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| DC                 | 9                     | PRAVEEN K. SAMUDRALA, Synthesis of SEU Tolerant FPGAs, January 22, 2003, pages 1-53.  |                |
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|--------------------|--------------------|-----------------|----------|
| Examiner Signature | <i>Paul D. Chy</i> | Date Considered | 12/29/04 |
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